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(54) **LIGHT EMITTING DIODE**

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Related U.S. Application Data

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(30) **Foreign Application Priority Data**

Dec. 3, 2011 (CN) 2011 1 0395475

(51) **Int. Cl.**

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H01L 33/24	(2010.01)
H01L 33/06	(2010.01)
H01L 33/22	(2010.01)
H01L 33/20	(2010.01)

(52) **U.S. Cl.**
CPC ***H01L 33/24*** (2013.01); ***H01L 33/06*** (2013.01); ***H01L 33/20*** (2013.01); ***H01L 33/22*** (2013.01)

(58) **Field of Classification Search**
CPC H01L 33/24; H01L 33/22; H01L 33/06; H01L 33/20
USPC 257/88, 99, 98, 100
See application file for complete search history.

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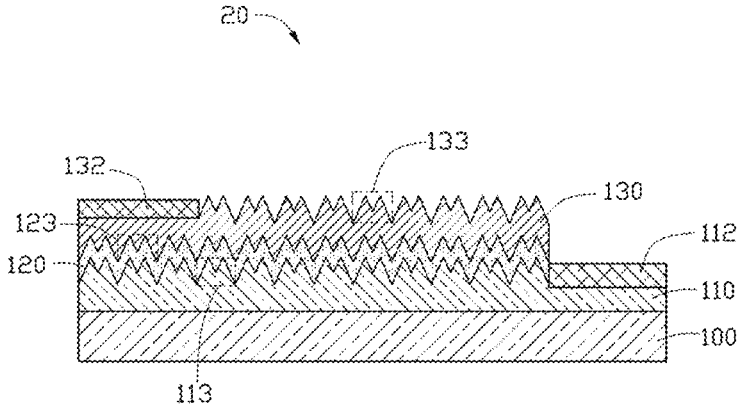
(57) **ABSTRACT**

A light emitting diode including a substrate, a first semiconductor layer, an active layer, and a second semiconductor layer is provided. The first semiconductor layer includes a first surface and a second surface. The active layer and the second semiconductor layer are stacked on the second surface in that order, and a surface of the second semiconductor layer away from the active layer is configured as the light emitting surface. A first electrode electrically is connected with the first semiconductor layer. A second electrode is electrically connected with the second semiconductor layer. A number of first three-dimensional nano-structures are located on the second surface of the first semiconductor layer. A number of second three-dimensional nano-structures are located on a surface of the active layer contacting the second semiconductor layer, and a cross section of each of the three-dimensional nano-structures is M-shaped.

20 Claims, 9 Drawing Sheets



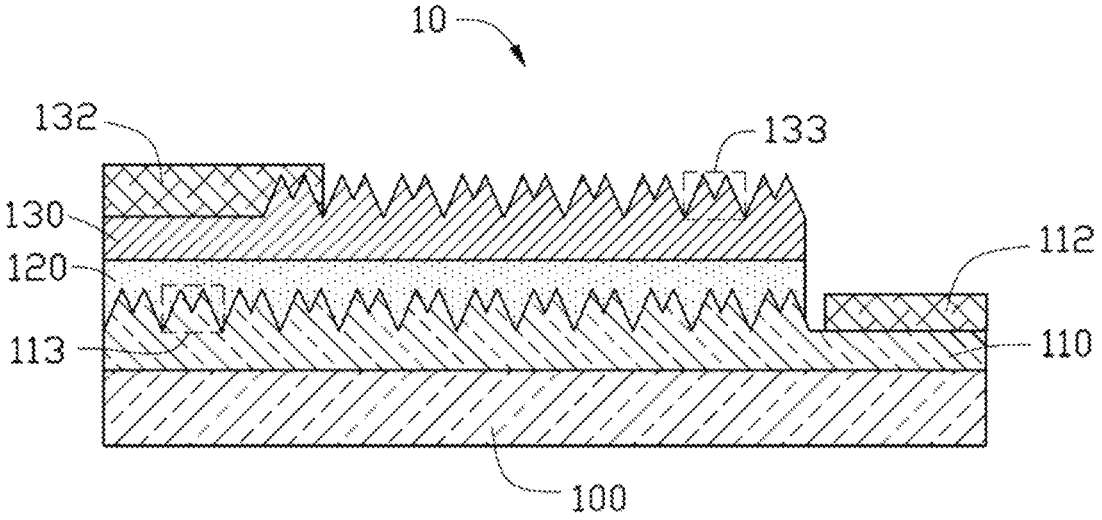


FIG. 1

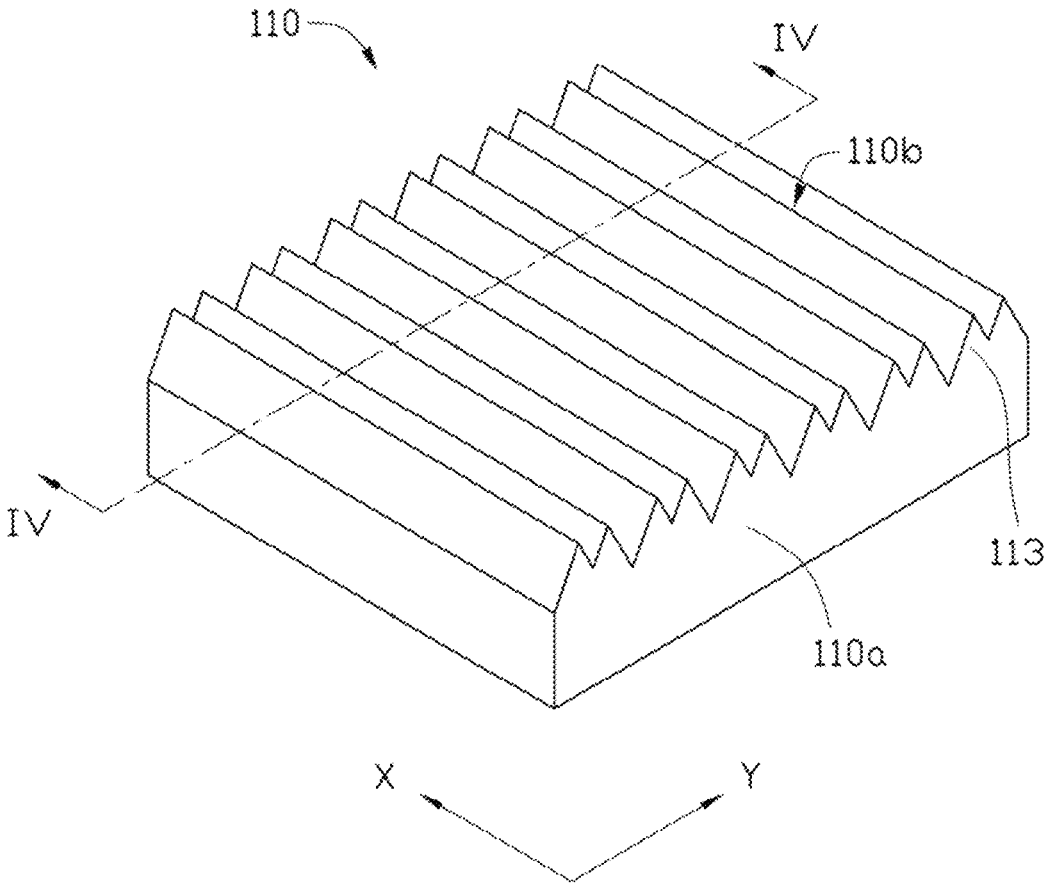


FIG. 2

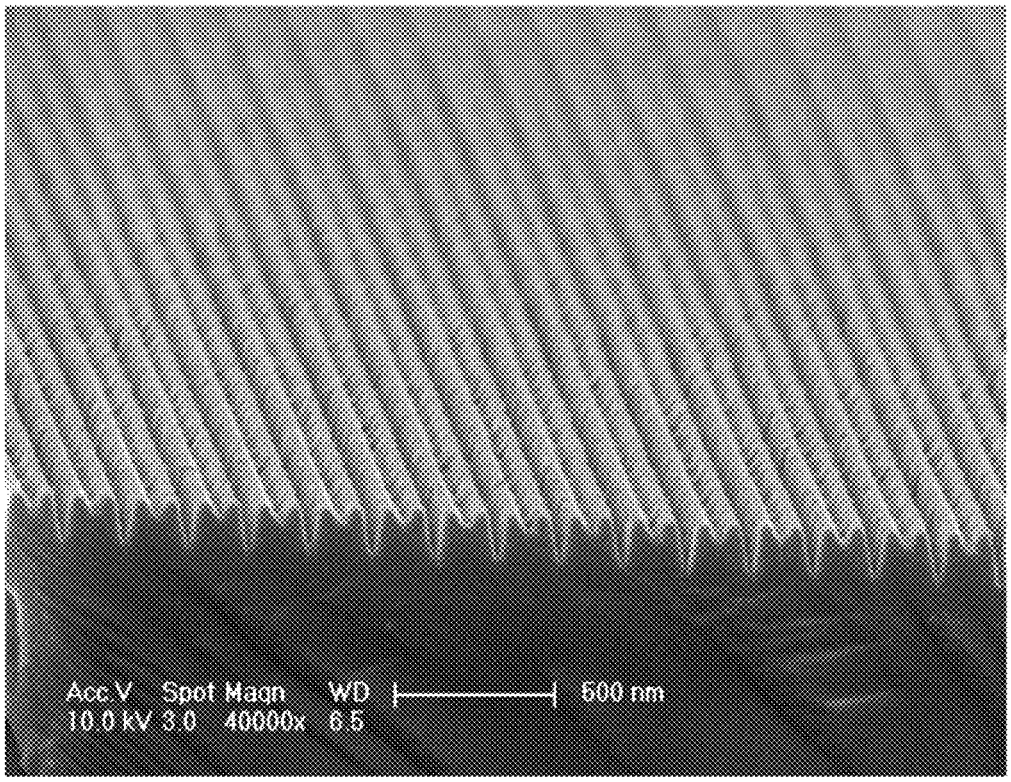


FIG. 3

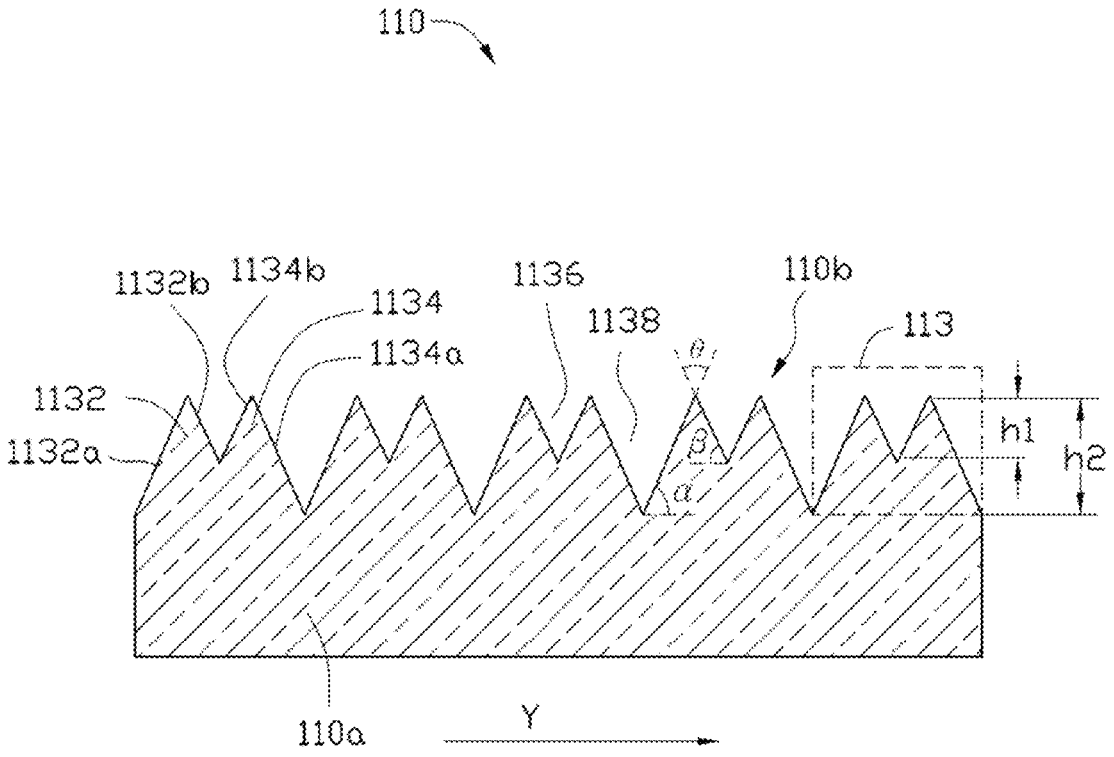

110
1132b
1134b
1134
1134a
1136
1138
110b
113
1132
1132a
θ
α
h1
h2
110a
Y

FIG. 4

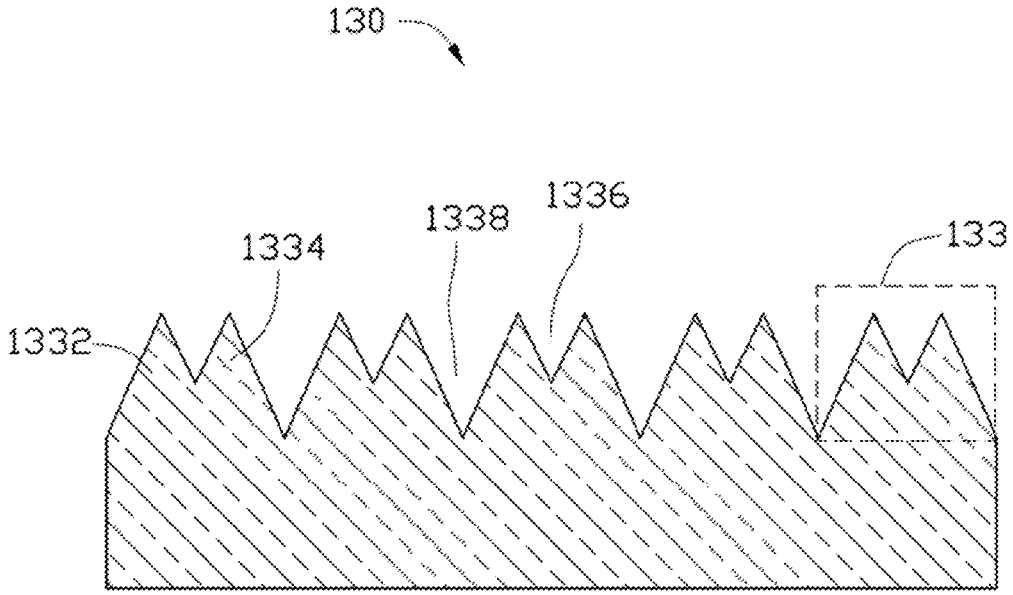


FIG. 5

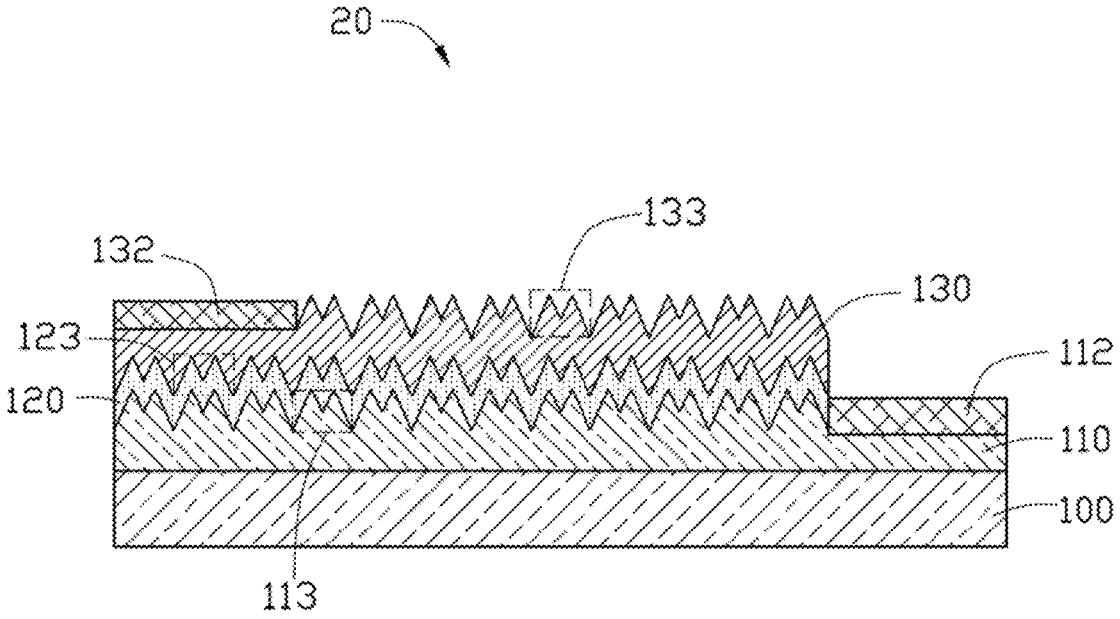


FIG. 6

FIG. 7

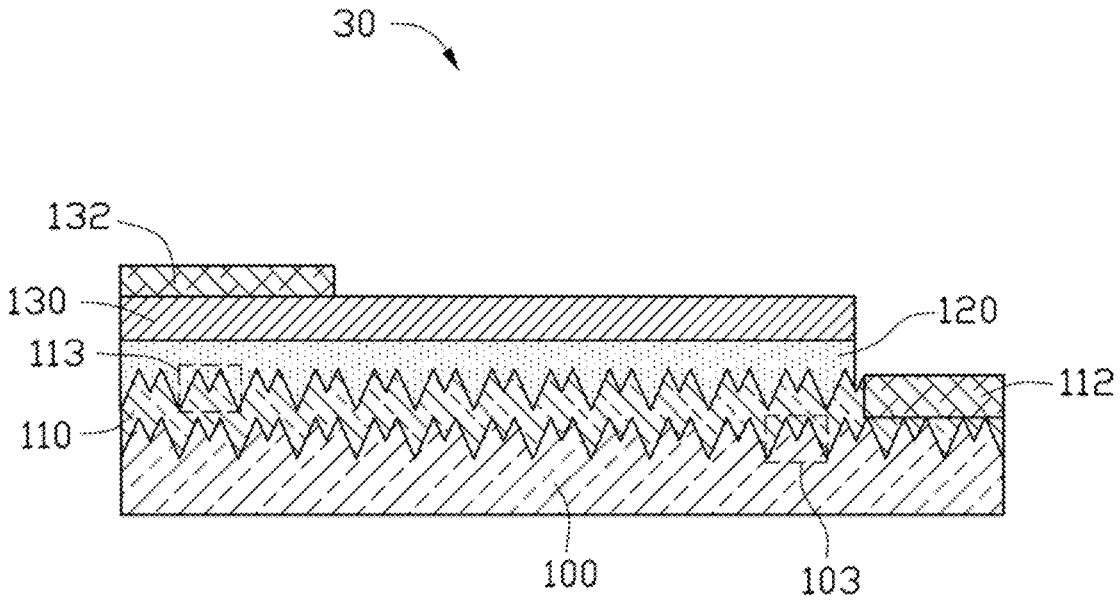


FIG. 8

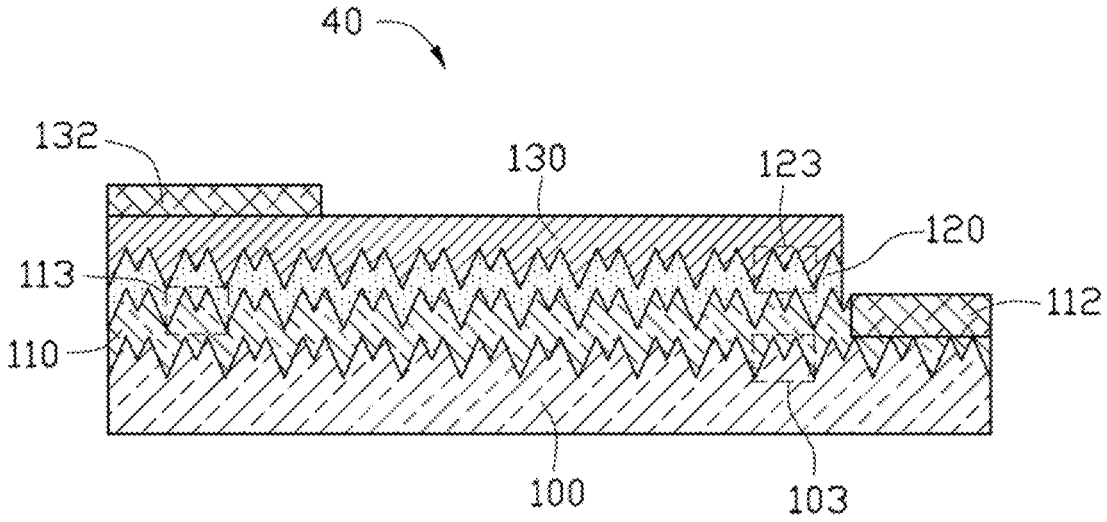


FIG. 9

LIGHT EMITTING DIODE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 14/096,159, filed on Dec. 4, 2013, entitled, "LIGHT EMITTING DIODE," which is a continuation of U.S. patent application Ser. No. 13/479,227, filed on May 23, 2012, entitled, "LIGHT EMITTING DIODE," which claims all benefits accruing under 35 U.S.C. §119 from China Patent Application No. 201110395475.1, filed on Dec. 3, 2011 in the China Intellectual Property Office. The disclosures of the above-identified applications are incorporated herein by reference.

BACKGROUND

1. Technical Field

The present disclosure relates to a light emitting diode (LED).

2. Description of the Related Art

LEDs are semiconductors that convert electrical energy into light. Compared to conventional light sources, LEDs have higher energy conversion efficiency, higher radiance (i.e., they emit a larger quantity of light per unit area), longer lifetime, higher response speed, and better reliability. LEDs also generate less heat. Therefore, LED modules are widely used as light sources in optical imaging systems, such as displays, projectors, and so on.

A typical LED commonly includes an N-type semiconductor layer, a P-type semiconductor layer, an active layer, an N-type electrode, and a P-type electrode. The active layer is located between the N-type semiconductor layer and the P-type semiconductor layer. The P-type electrode is located on the P-type semiconductor layer. The N-type electrode is located on the N-type semiconductor layer. Typically, the P-type electrode is transparent. In operation, a positive voltage and a negative voltage are applied respectively to the P-type semiconductor layer and the N-type semiconductor layer. Thus, holes in the P-type semiconductor layer and photons in the N-type semiconductor layer can enter the active layer and combine with each other to emit visible light.

However, the extraction efficiency of LEDs is low because the contact area between the N-type semiconductor layer and the active layer is not large enough. Thus the electron-hole recombination density is low, and the photons in the LED are sparse, thereby degrading the extraction efficiency.

What is needed, therefore, is a light emitting diode which can overcome the above-described shortcomings.

BRIEF DESCRIPTION OF THE DRAWINGS

Many aspects of the embodiments can be better understood with reference to the following drawings. The components in the drawings are not necessarily drawn to scale, the emphasis instead being placed upon clearly illustrating the principles of the embodiments. Moreover, in the drawings, like reference numerals designate corresponding parts throughout the several views.

FIG. **1** shows a schematic view of one embodiment of an LED.

FIG. **2** is an isometric view of one embodiment of a three-dimensional nano-structures array in the LED of FIG. **1**.

FIG. **3** shows a scanning electron microscope (SEM) image of the three-dimensional nano-structures array of FIG. **2**.

FIG. **4** shows cross-sectional view along a line IV-IV of FIG. **2**.

FIG. **5** shows a schematic view of the second semiconductor layer of FIG. **1**.

FIG. **6** shows a schematic view of another embodiment of an LED.

FIG. **7** shows a schematic view of the active layer of FIG. **6**.

FIG. **8** shows a schematic view of another embodiment of an LED.

FIG. **9** shows a schematic view of another embodiment of an LED.

DETAILED DESCRIPTION

The disclosure is illustrated by way of example and not by way of limitation in the figures of the accompanying drawings in which like references indicate similar elements. It should be noted that references to "an" or "one" embodiment in this disclosure are not necessarily to the same embodiment, and such references mean at least one.

Referring to FIG. **1**, an LED **10** includes a substrate **100**, a first semiconductor layer **110**, an active layer **120**, a second semiconductor layer **130**, a first electrode **112**, and a second electrode **132**. The first semiconductor layer **110** includes a first surface and the second surface opposite to the first surface. The substrate **100** contacts with the first surface of the first semiconductor layer **110**. The active layer **120** and the second semiconductor layer **130** are stacked on the second surface of the first semiconductor layer **110**, and in that order. The surface of the second semiconductor layer **130** away from the active layer **120** is configured as the light emitting surface of LED **10**. The second surface of the first semiconductor layer **110** defines a plurality of three-dimensional nano-structures **113**. The light emitting surface of the LED **10** defines a plurality of three-dimensional nano structures **133**. The first electrode **112** is electrically connected with the first semiconductor layer **110**, and the second electrode **132** is electrically connected with the second semiconductor layer **130**.

The substrate **100** can be made of a transparent material and adapted to support the first semiconductor layer **110**. A shape or a size of the substrate **100** is determined according to need. The substrate **100** includes an epitaxial growth surface **101** which is used to grow the first semiconductor layer **110**. The epitaxial growth surface **101** is a clean and smooth surface. The substrate **100** can be a single-layer structure or a multi-layer structure. If the substrate **100** is a single-layer structure, the substrate **100** can be a single crystal structure having a crystal face used as the epitaxial growth surface **101**. If the substrate **100** is a multi-layer structure, the substrate **100** should include at least one layer having the crystal face. The material of the substrate **100** can be GaAs, GaN, AlN, Si, SOI, SiC, MgO, ZnO, $LiGaO_2$, $LiAlO_2$, or Al_2O_3. The first semiconductor layer **110** and the substrate **100** should have a small crystal lattice mismatch and a thermal expansion mismatch. The size, thickness, and shape of the substrate **100** can be selected according to need. In one embodiment, the substrate **100** is a sapphire substrate with a thickness of about 40 nm.

The first semiconductor layer **110** is formed on the epitaxial growth surface **101**. The first semiconductor layer **110** is an N-type semiconductor or a P-type semiconductor. The material of the N-type semiconductor can include N-type gallium nitride, N-type gallium arsenide, or N-type copper phosphate. The material of the P-type semiconductor can include P-type gallium nitride, P-type gallium arsenide, or

P-type copper phosphate. The N-type semiconductor is configured to provide photons, and the P-type semiconductor is configured to provide holes. The thickness of the first semiconductor layer **110** ranges from about 1 μm to about 5 μm. In one embodiment, the first semiconductor layer **110** is an N-type gallium nitride doped with Si. The first semiconductor layer **110** includes a first surface and a second surface opposite to the first surface. The first surface is contacted with the substrate **100**. The second surface includes a first region and a second region based on their function. The first region is used to locate the active layer **120** and the second semiconductor layer **130**, and the second region is used to locate the first electrode **112**.

In one embodiment, a buffer layer (not shown) can be sandwiched between the substrate **100** and the first semiconductor layer **110**. Because the first semiconductor layer **110** and the substrate **100** have different lattice constants, the buffer layer is used to reduce the lattice mismatch, thus the dislocation density of the first semiconductor layer **110** will decrease. The thickness of the buffer layer ranges from about 10 nanometers to about 300 nanometers, and the material of the buffer layer can be GaN or AlN.

Referring to FIG. **1** and FIG. **2**, the second surface of the first semiconductor layer **110** is a patterned surface. The first semiconductor layer **110** can be separated into a main body **110***a* and a protruding part **110***b* and distinguished by an "interface." The interface can be parallel with the first surface of the first semiconductor layer **110**. The interface is defined as a surface of the main body **110***a* hereafter, and the protruding part **110***b* extends away from the surface of the main body **110***a*. The protruding part **110***b* defines the plurality of three-dimensional nano-structures **113**, and the plurality of three-dimensional nano-structures **113** form the patterned surface of the first semiconductor layer **110**. The three-dimensional nano-structure **113** can be a protruding structure. The protruding structure protrudes out from the interface of the main body **110***a*. The plurality of three-dimensional nano-structures **113** is a protruding structure located on the surface of the main body **110***a*.

The plurality of three-dimensional nano-structures **113** can be arranged side by side. Each of the three-dimensional nano-structures **113** can extend along a straight line, a curvy line, or a polygonal line. The extending direction is substantially parallel with the surface of the first semiconductor layer **110**. The two adjacent three-dimensional nano-structures are arranged a certain distance apart from each other. The distance ranges from about 0 nanometers to about 1000 nanometers, such as 10 nanometers, 30 nanometers, or 200 nanometers. The extending direction of the three-dimensional nano-structure **113** can be fixed or varied. While the extending direction of the three-dimensional nano-structure **113** is fixed, the plurality of three-dimensional nano-structures **113** extends along a straight line, otherwise the three-dimensional nano-structures **113** extends along a polygonal line or a curvy line. The cross-section of the three-dimensional nano-structure **113** along the extending direction is M-shaped. Referring to FIG. **3**, the three-dimensional nano-structures **113** are a plurality of substantially parallel bar-shaped protruding structures extending along a straight line. The plurality of three-dimensional nano-structures **113** are substantially uniformly and equidistantly distributed on the entire surface of the main body **110***a*.

Also referring to FIG. **4**, the three-dimensional nano-structure **113** extends from one side of the semiconductor layer **110** to the opposite side along the X direction. The Y direction is substantially perpendicular to the X direction and substantially parallel with the surface of the main body **110***a*. The three-dimensional nano-structure **113** is a double-peak structure including two peaks. The cross-section of the double-peak structure is in the shape of an M. The first peak **1132** and the second peak **1134** substantially extend along the X direction. The first peak **1132** includes a first surface **1132***a* and a second surface **1132***b*. The first surface **1132***a* and the second surface **1132***b* intersect to form an intersection line and an included angle θ of the first peak **1132**. The intersection line can be a straight line, a curvy line, or a polygonal line. The included angle θ is greater than 0 degree and smaller than 180 degrees. In one embodiment, the included angle θ ranges from about 30 degrees to about 90 degrees. The first surface **1132***a* and the second surface **1132***b* can be planar, curvy, or wrinkly. In one embodiment, the first surface **1132***a* and the second surface **1132***b* are planar. The first surface **1132***a* intersects the surface of the main body **110***a* at an angle α. The angle α is greater than 0 degrees and less than or equal to 90 degrees. In one embodiment, the angle α is greater than 80 degrees and less than 90 degrees. The first surface **1132***a* includes a side connected to the surface of the substrate **100**, and extends away from the main body **110***a* to intersect the second surface **1132***b*. The second surface **1132***b* includes a side connected with the second peak **1134** and extends away from the main body **110***a* at an angle β. The angle β is greater than 0 degrees and smaller than 90 degrees.

The second peak **1134** includes a third surface **1134***a* and a fourth surface **1134***b*. The structure of the second peak **1134** is substantially the same as that of the first peak **1132**. The third surface **1134***a* and the fourth surface **1134***b* intersect each other to form the included angle of the second peak **1134**. The third surface **1134***a* includes a side intersected with the surface of the main body **110***a*, and extends away from the main body **110***a* to intersect with the fourth surface **1134***b*. The fourth surface **1134***b* includes a side intersecting the third surface **1134***a* to form the included angle of the second peak **1134**, and extends to intersect the second surface **1132***b* of the first peak **1132** to define a first groove **1136**. A second groove **1138** is defined between two adjacent three-dimensional nano-structures **113**. The second groove **1138** is defined by the third surface **1134***a* of the second peak **1134** and the first surface **1132***a* of the first peak **1132** of the adjacent three-dimensional nano-structure **113**.

The first peak **1132** and the second peak **1134** protrude out of the main body **110***a*. The height of the first peak **1132** and the second peak **1134** is arbitrary and can be selected according to need. In one embodiment, both the height of the first peak **1132** and that of the second peak **1134** range from about 150 nanometers to about 200 nanometers. The height of the first peak **1132** can be substantially equal to that of the second peak **1134**. The highest points of the first peak **1132** and the second peak **1134** are defined as the farthest point away from the surface of the main body **110***a*. In one three-dimensional nano-structure **113**, the highest point of the first peak **1132** is spaced from that of the second peak **1134** a certain distance ranging from about 20 nanometers to about 100 nanometers. The first peak **1132** and the second peak **1134** extend substantially along the X direction. The cross-section of the first peak **1132** and the second peak **1134** can be trapezoidal or triangular, and the shape of the first peak **1132** and the second peak **1134** can be substantially the same. In one embodiment, the cross-sections of the first peak **1132** and the second peak **1134** are triangular. In one embodiment, the first peak **1132**, the second peak **1134**, and the main body **110***a* form an integrated structure. Because of the limitation of the technology, the first surface **1132***a* and the second surface **1132***b* cannot be absolutely planar.

In each M-shaped three-dimensional nano-structure **113**, the first peak **1132** and the second peak **1134** define the first groove **1136**. The extending direction of the first groove **1136** is substantially the same as the extending direction of the first peak **1132** and the second peak **1134**. The cross-section of the first groove **1136** is V-shaped. The depth h_1 of the first groove **1136** in different three-dimensional nano-structures **113** is substantially the same. The depth h_1 is defined as the distance between the highest point of the first peak **1132** and the lowest point of the first groove **1136**. The depth of the first groove **1136** is less than the height of the first peak **1132** and the second peak **1134**.

The second groove **1138** extends substantially along the extending direction of the three-dimensional nano-structures **113**. The cross-section of the second groove **1138** is V-shaped or an inverse trapezium. Along the extending direction, the cross-section of the second groove **1138** is substantially the same. The depth h_2 of the second grooves **1138** between each two adjacent three-dimensional nano-structures **113** is substantially the same. The depth h_2 is defined as the distance between the highest point and the lowest point of the groove of the second groove **1138**. The depth of the second groove **1138** is greater than the depth of the first groove **1136**, and the ratio between h_1 and h_2 ranges from about 1:1.2 to about 1:3 ($1:1.2 \leq h_1:h_2 \leq 1:3$). The depth of the first groove **1136** ranges from about 30 nanometers to about 120 nanometers, and the depth of the second groove **1138** ranges from about 90 nanometers to about 200 nanometers. In one embodiment, the depth of the first groove **1136** is about 80 nanometers, and the depth of the second groove **1138** is about 180 nanometers. The depth of the first groove **1136** and the second groove **1138** can be selected according to need.

The width of the three-dimensional nano-structure **113** ranges from about 100 nanometers to about 200 nanometers. The width of the three-dimensional nano-structure **113** is defined as the maximum span of the three-dimensional nano-structure **113** along the Y direction. The span of the three-dimensional nano-structure **113** gradually decreases along the direction away from the substrate **100**. Thus in each three-dimensional nano-structure **113**, the distance between the highest point of the first peak **1132** and the highest point of the second peak **1134** is less than the width of the three-dimensional nano-structure **113**. The plurality of three-dimensional nano-structures **113** can be distributed in a certain interval from each other, and the intervals can be substantially the same. The interval forms the second groove **1138**. The distance λ_0 between the two adjacent three-dimensional nano-structures **120** ranges from about 0 nanometers to about 200 nanometers. The distance between each two adjacent three-dimensional nano-structures **120** can be substantially the same. The distance λ_0 can be increased with the increase of the height of both the first peak **1132** and second peak **1134**, and decreased with the decrease of the height of both the first peaks **1132** and second peaks **1134**. In the Y direction, the distance λ_0 can be increased, decreased, or periodically varied. If the distance $\lambda_0=0$, the cross-section of the second groove **1138** is V-shaped. If the distance $\lambda_0>0$, the cross-section of the second groove **1138** is in the shape of an inverse trapezium.

Along the Y direction, the plurality of three-dimensional nano-structures **113** is distributed in a certain period P. One period P is defined as the width λ of the three-dimensional nano-structures **113** added with the distance λ_0. The period P of the plurality of three-dimensional nano-structures **113** can range from about 100 nanometers to about 500 nanometers. The period P, the width λ, and the distance λ_0 satisfy the following formula: $P=\lambda+\lambda_0$. The period P, the width λ, and the distance λ_0 is measured in nanometers. The period P can be a constant, and λ_0 or λ can be a dependent variable. Furthermore, one part of the three-dimensional nano-structures **113** can be aligned in a first period, and another part of the three-dimensional nano-structures **113** can be aligned in a second period. In one embodiment, the period P is about 200 nanometers, the width λ is about 190 nanometers, and the distance λ_0 is about 10 nanometers.

The active layer **120** is located on the first region of the second surface of the first semiconductor layer **110**. In one embodiment, the active layer **120** covers the entire surface of the first region. The active layer **120** is engaged with the first semiconductor layer **110**. In detail, the active layer **120** covers the plurality of three-dimensional nano-structures **113**, and the surface of the active layer **120** which is connected with the first semiconductor layer **110** forms a patterned surface. The active layer **120** also includes a plurality of third grooves and third peaks, the grooves being engaged with the first peaks **1132** and second peaks **1134**, the peaks being engaged with the first grooves **1136** and second grooves **1138**. The active layer **120** is a photon excitation layer and can be one of a single layer quantum well film or multilayer quantum well films. The active layer **120** is made of GaInN, AlGaInN, GaSn, AlGaSn, GaInP, or GaInSn. In one embodiment, the active layer **120** has a thickness of about 0.3 μm and includes one layer of GaInN and another layer of GaN. The GaInN layer is stacked with the GaN layer.

Referring also to FIG. **5**, the second semiconductor layer **130** is located on the active layer **120**. The surface of the second semiconductor layer **130** away from the active layer **120** is configured as the light emitting surface of LED **10**. In one embodiment, the second semiconductor layer **130** covers the entire surface of the active layer **120** away from the substrate **100**. The thickness of the second semiconductor layer **130** ranges from about 0.1 μm to about 3 μm. The second semiconductor layer **130** can be an N-type semiconductor layer or a P-type semiconductor layer. Furthermore, the type of the second semiconductor layer **130** is different from the type of the first semiconductor layer **110**. In one embodiment the second semiconductor layer **130** is a P-type gallium nitride doped with Mg. Furthermore, the light emitting surface of the LED **10** defines the plurality of three-dimensional nano-structures **133** to form a patterned surface. The structure of the three-dimensional nano-structures **133** is the same as the structure of the three-dimensional nano-structures **113**. The three-dimensional nano-structure **133** is a protruding structure extending away from the second semiconductor layer **130**. The plurality of three-dimensional nano-structures **133** can be arranged side by side. The extending direction of the three-dimensional nanostructures **133** can be fixed or varied. The cross-section of the three-dimensional nanostructure **133** along the extending direction is M-shaped. Each M-shaped three-dimensional nano-structure **133** includes a first peak **1332** and a second peak **1334** extending along the same direction. A first groove **1336** is defined between the first peak **1332** and the second peak **1334**. A second groove **1338** is defined between the two adjacent three-dimensional nano-structures **133**. The depth of the first groove **1336** is smaller than the depth of the second groove **1338**.

The first electrode **112** is electrically connected with the first semiconductor layer **110** and spaced from the active layer **120**. The first electrode **112** covers at least part of the surface of the second region. The first electrode **112** is a single layer structure or a multi-layer structure. The first electrode **112** can be an N-type electrode or a P-type electrode depending on the first semiconductor layer **110**. The material of the first electrode **112** can be titanium (Ti), silver (Ag), aluminum (Al),

nickel (Ni), gold (Au), or any combination of them. The material of the first electrode **112** can also be indium-tin oxide (ITO) or carbon nanotube film. In one embodiment, the first electrode **112** is a two-layer structure consisting of a Ti layer with a thickness of about 15 nm and an Au layer with a thickness of about 100 nm.

The second electrode **132** can be an N-type electrode or P-type electrode. In one embodiment, the second electrode **132** is located on the light emitting surface of LED **10**. In detail, the second electrode **132** covers at least part of the three-dimensional nano-structures **133**. The type of the second electrode **132** is the same as the second semiconductor layer **130**. The shape of the second electrode **132** is arbitrary and can be selected according to need. The second electrode **132** covers a part of the surface or the entire surface of the second semiconductor layer **130**. The material of the second electrode **132** can be Ti, Ag, Al, Ni, Au, or any combination of them.

Furthermore, a reflector layer (not shown) can be located on the surface of substrate **100** away from the active layer **120**. The material of the reflector can be Ti, Ag, Al, Ni, Au, or any combination thereof. The reflector includes a smooth surface having a high reflectivity. The photons reach the reflector and will be reflected by the reflector, thus these photons can be extracted out of the LED **10** to improve the light extraction efficiency of the LED **10**.

The first semiconductor layer **110** includes a plurality of three-dimensional nano-structures to form a patterned surface, and the active layer **120** is located on the patterned surface, thus the contact area between the first semiconductor layer **110** and the active layer **120** is enlarged. The electron-hole recombination density is improved, and the quantity of photons is increased. The light extraction efficiency of the LED **10** can be improved.

One embodiment of a method for making the LED **10** includes the following steps:

S**11**, providing a substrate **100** with an epitaxial growth surface **101**;

S**12**, growing a first semiconductor layer **110** on the epitaxial growth surface **101**;

S**13**, forming a plurality of three-dimensional nano-structures **113** on the first semiconductor layer **110**;

S**14**, growing an active layer **120** and a second semiconductor layer **130** on the surface of the plurality of three-dimensional nano-structures **113** in that order;

S**15**, forming a plurality of three-dimensional nano-structures **133** by etching the surface of the second semiconductor layer **130** away from the active layer **120**;

S**16**, applying a first electrode **112** electrically connected to the first semiconductor layer **110**; and

S**17**, locating a second electrode **132** electrically connected to the second semiconductor layer **130**.

Referring to FIG. **6**, another embodiment of an LED **20** includes a substrate **100**, a first semiconductor layer **110**, an active layer **120**, a second semiconductor layer **130**, a first electrode **112**, and a second electrode **132**. The first semiconductor layer **110** includes a first surface and an opposite second surface. The first surface is in contact with the substrate **100**. The active layer **120** and the second semiconductor layer **130** are stacked on the second surface and in that order. The surface of the second semiconductor layer **130** away from the active layer **120** is configured as the light emitting surface of the LED **10**. The second surface of the first semiconductor layer defines a plurality of three-dimensional nano-structures **113**. The surface of the active layer **120** away from the first semiconductor layer **110** defines a plurality of three-dimensional nano-structures **123**. The light emitting surface of the LED **10** defines a plurality of three-dimensional nano-structures **133**. The first electrode **112** is electrically connected with the first semiconductor layer **110**, and the second electrode **132** is electrically connected with the second semiconductor layer **130**. The plurality of three-dimensional nano-structures **123** is located on the surface of the active layer **120** away from the first semiconductor layer **110**. The structure of the LED **20** is similar to that of the LED **10**, except that a plurality of three-dimensional nano-structures **123** are located on the active layer **120** away form the first semiconductor layer **110**.

Referring to FIG. **7**, the plurality of three-dimensional nano-structures **123** forms a patterned surface on the active layer **120**. The three-dimensional nano-structure **123** is similar to the three-dimensional nano-structures **113**. Each three-dimensional nano-structure **123** includes a first peak **1232**, a second peak **1234**, a first groove **1236** defined between the first peak **1232** and the second peak **1234**, and a second groove **1238** defined between two adjacent three-dimensional nano-structures **123**. The distribution and alignment of the three-dimensional nano-structures **123** is the same as the distribution and alignment of the three-dimensional nano-structures **113**. The second semiconductor layer **130** is located on the surface of the three-dimensional nano-structures **113**, thus the surface of the second semiconductor layer **130** near the active layer **120** forms a patterned surface.

In the LED **20**, the surface of the second semiconductor layer **130** in contact with the active layer **120** also includes a plurality of three-dimensional nano-structures **123**, thus the contact area between the semiconductor layer and the active layer is also enlarged. The electron-hole recombination density is further increased, and the light extraction efficiency of the LED **20** can be improved.

One embodiment of a method for making the LED **20** includes the following steps:

S**21**, providing a substrate **100** having an epitaxial growth surface **101**;

S**22**, growing a first semiconductor layer **110**;

S**23**, forming a plurality of three-dimensional nano-structures **113** on a surface of the semiconductor layer **110**;

S**24**, growing an active layer **120** on the surface of the three-dimensional nano-structures **113**, and forming a plurality of three-dimensional nano-structures **123** on the surface which is away from the first semiconductor layer **110**;

S**25**, growing a second semiconductor layer **130** on the surface of three-dimensional nano-structures **123**;

S**26**, forming a plurality of three-dimensional nano-structures **133** on the surface of the semiconductor layer **130**;

S**27**, applying a first electrode **112** on the surface of the first semiconductor layer **110**; and

S**28**, applying a second electrode **132** electrically connected to the second semiconductor layer **130**.

The method of making the LED **20** is similar to the method for making the LED **10**, except that the LED **20** further forms the plurality of three-dimensional nano-structures **123** on the surface of the active layer **120** away from the first semiconductor layer **110**. The substrate **100** with the first semiconductor layer **110** is located in a vertical epitaxial growth reactor, and the active layer **120** grows by a vertical epitaxial growth method. Thus the distribution and alignment of the three-dimensional nano-structure **123** can be the same as the distribution and alignment of the three-dimensional nano-structure **113**.

Referring to FIG. **8**, another embodiment of an LED **30** includes a substrate **100**, a first semiconductor layer **110**, an active layer **120**, a second semiconductor layer **130**, a first electrode **112**, and a second electrode **132**. The first semicon-

ductor layer **110** includes a first surface and the second surface opposite to the first surface. The substrate **100** contacts the first surface of the first semiconductor layer **110**. The active layer **120** and the second semiconductor layer **130** are stacked on the second surface of the first semiconductor layer **110**, and in that order. The surface of the second semiconductor layer **120** away from the active layer **120** is configured as the light emitting surface of the LED **10**. The second surface of the first semiconductor layer **110** defines a plurality of three-dimensional nano-structures **113**. The surface of the substrate **100** contacting the first semiconductor layer **110** defines a plurality of three-dimensional nano-structures **103**. The first electrode **112** is electrically connected with the first semiconductor layer **110**, and the second electrode **132** is electrically connected with the second semiconductor layer **130**. The structure of the LED **30** is similar to the structure of the LED **10**, except that the LED **30** further includes the plurality of three-dimensional nano-structures **103** located on the surface of the substrate **100** which contacts the first semiconductor layer **110**.

The plurality of three-dimensional nano-structures **103** forms a patterned surface. The three-dimensional nano-structure **103** is similar to the three-dimensional nano-structures **113**. The distribution and alignment of the three-dimensional nano-structures **103** is the same as that of the three-dimensional nano-structures **113**. The first semiconductor layer **110** is located on the surface of the three-dimensional nano-structures **103**, thus the surface of the first semiconductor layer **110** near the substrate **100** forms a patterned surface.

One embodiment of a method for making the LED **30** includes the following steps:

S**31**, providing a substrate **100**;

S**32**, forming a plurality of three-dimensional nano-structures **103** on a surface of the substrate **100** to form a patterned epitaxial growth surface **101**;

S**33**, growing a first semiconductor layer **110** on the patterned epitaxial growth surface **101**;

S**34**, forming a plurality of three-dimensional nano-structures **113** on a surface of the semiconductor layer **110**;

S**35**, growing an active layer **120** and a second semiconductor layer **130** on the surface of three-dimensional nano-structures **113**;

S**36**, applying a first electrode **112** on the surface of the first semiconductor layer **110**; and

S**37**, applying a second electrode **132** electrically connected to the second semiconductor layer **130**.

Photons reaching the plurality of three-dimensional nano-structures **103** with a large incident angle can be reflected, changing the direction of the moving photons so that the photons can be extracted from the light emitting surface. Furthermore, because the three-dimensional nano-structure **103** is M-shaped, the three-dimensional nano-structures **103** function as two layers of three-dimensional nano-structures assembled together, and the light extraction efficiency of the LED **30** will be improved.

Referring to FIG. **9**, another embodiment of an LED **40** includes a substrate **100**, a first semiconductor layer **110**, an active layer **120**, a second semiconductor layer **130**, a first electrode **112**, and a second electrode **132**. The first semiconductor layer **110** includes a first surface and the second surface opposite to the first surface. The substrate **100** contacts the first surface of the first semiconductor layer **110**. The active layer **120** and the second semiconductor layer **130** are stacked on the second surface of the first semiconductor layer **110** in that order. The surface of the second semiconductor layer **120** away from the active layer **120** is configured as the light emitting surface of the LED **10**. The second surface of the first semiconductor layer **110** defines a plurality of three-dimensional nano-structures **113**. The surface of the active layer **120** away from the first semiconductor layer **110** defines a plurality of three-dimensional nano-structures **123**. The surface of the substrate **100** contacting the first semiconductor layer **110** defines a plurality of three-dimensional nano-structures **103**. The first electrode **112** is electrically connected with the first semiconductor layer **110**, and the second electrode **132** is electrically connected with the second semiconductor layer **130**. The structure of the LED **40** is similar to the structure of the LED **30**, except the LED **40** further includes the plurality of three-dimensional nano-structures **123** located on the surface of the active layer **120** away from the first semiconductor **110**.

The three-dimensional nano-structure **123** is similar to the three-dimensional nano-structures **113**. The distribution and alignment of the three-dimensional nano-structures **123** is the same as the distribution and alignment of the three-dimensional nano-structures **113**.

Depending on the embodiment, certain of the steps of methods described may be removed, others may be added, and the sequence of steps may be altered. It is also to be understood that the description and the claims drawn to a method may include some indication in reference to certain steps. However, the indication used is only to be viewed for identification purposes and not as a suggestion as to an order for the steps.

It is to be understood that the above-described embodiments are intended to illustrate rather than limit the disclosure. Variations may be made to the embodiments without departing from the spirit of the disclosure as claimed. It is understood that any element of any one embodiment is considered to be disclosed to be incorporated with any other embodiment. The above-described embodiments illustrate the scope of the disclosure but do not restrict the scope of the disclosure.

What is claimed is:

1. A light emitting diode, comprising:

a substrate;

a first semiconductor layer comprising a first surface contacting the substrate and a second surface opposite to the first surface;

an active layer stacked on the second surface of the first semiconductor layer;

a second semiconductor layer stacked on the active layer and comprising a light emitting surface away from the active layer;

a first electrode electrically connected with the first semiconductor layer;

a second electrode electrically connected with the second semiconductor layer;

wherein a plurality of first three-dimensional nano-structures are located on the second surface of the first semiconductor layer, a plurality of second three-dimensional nano-structures are located on a surface of the active layer contacting the second semiconductor layer, wherein each of the plurality of first three-dimensional nano-structures and the plurality of second three-dimensional nano-structures comprises a first peak and a second peak, a first groove is defined between the first peak and the second peak, a second groove is defined between adjacent two of the plurality of first three-dimensional nano-structures and adjacent two of the plurality of second three-dimensional nano-structures, and a depth of the first groove is less than a depth of the second groove.

2. The light emitting diode of claim **1**, wherein a surface of the active layer adjacent to the first semiconductor layer is

engaged with the plurality of first three-dimensional nano-structures on the first semiconductor layer to form a first patterned surface.

3. The light emitting diode of claim **1**, wherein the active layer is in contact with and covers the plurality of first three-dimensional nano-structures.

4. The light emitting diode of claim **1**, wherein the each of the plurality of first three-dimensional nano-structures is a bar-shaped protruding structure extending along a straight line, a curve line, or a polygonal line.

5. The light emitting diode of claim **1**, wherein a cross-section of each of the plurality of first three-dimensional nano-structures is M-shaped.

6. The light emitting diode of claim **1**, wherein the first peak comprises a first surface and a second surface, the first surface intersects with the second surface to define a first include angle, the second peak comprises a third surface and a fourth surface, the third surface intersects with the fourth surface to form a second include angle, and the first include angle and the second include angle range from about 30 degrees to about 90 degrees.

7. The light emitting diode of claim **1**, wherein a cross-section of the first peak is trapezoid shaped or triangle shaped, and a cross-section of the second peak is trapezoid shaped or a triangle shaped.

8. The light emitting diode of claim **1**, wherein a depth of the first groove ranges from about 30 nanometers to about 120 nanometers, and a depth of the second groove ranges from about 100 nanometers to about 200 nanometers.

9. The light emitting diode of claim **1**, wherein the plurality of first three-dimensional nano-structures are side by side joined to form a plurality of concentric circles or concentric rectangles.

10. The light emitting diode of claim **1**, wherein the plurality of first three-dimensional nano-structures is aligned at an interval ranging from about 100 nanometers to about 500 nanometers.

11. The light emitting diode of claim **1**, wherein a distance between adjacent two of the plurality of first three-dimensional nano-structures ranges from about 0 nanometers to about 200 nanometers.

12. The light emitting diode of claim **1**, wherein a width of each of the plurality of first three-dimensional nano-structures ranges from about 100 nanometers to about 300 nanometers.

13. The light emitting diode of claim **1**, wherein a surface of the first semiconductor layer away from the substrate comprises a first region and a second region, the second semiconductor layer and the active layer are located on the first region, the second region is exposed from the second semiconductor layer and the active layer, and the first electrode is located on the second region.

14. The light emitting diode of claim **1**, wherein a surface of the second semiconductor layer is engaged with the plurality of second three-dimensional nano-structures to form a second patterned surface.

15. The light emitting diode of claim **1**, further comprising a plurality of third three-dimensional nano-structures located on the surface of the second semiconductor layer away from the substrate.

16. The light emitting diode of claim **15**, wherein the plurality of third three-dimensional nano-structures, the plurality of second three-dimensional nano-structures, and the plurality of first three-dimensional nano-structures are distributed with a same concentration and a same alignment.

17. A light emitting diode, comprising:

a substrate;

a first semiconductor layer comprising a first surface contacting the substrate and a second surface opposite to the first surface;

an active layer stacked on the second surface of the first semiconductor layer;

a second semiconductor layer stacked on the active layer and comprising a light emitting surface away from the active layer;

a first electrode electrically connected with the first semiconductor layer;

a second electrode electrically connected with the second semiconductor layer;

wherein each of two opposite surfaces of the active layer comprises a plurality of three-dimensional nano-structures, and a cross section of each of the plurality of three-dimensional nano-structures is M-shaped.

18. A light emitting diode, comprising:

a substrate comprising an epitaxial growth surface;

a first semiconductor layer stacked on the substrate;

an active layer stacked on the substrate;

a second semiconductor layer stacked on the active layer and comprising a light emitting surface away from the active layer;

a first electrode electrically connected with the first semiconductor layer;

a second electrode electrically connected with the second semiconductor layer;

a plurality of first three-dimensional nano-structures on the epitaxial growth surface;

a plurality of second three-dimensional nanostructures on a surface of the first semiconductor layer away from the substrate; and

a plurality of third three-dimensional nanostructures on a surface of the second semiconductor layer away from the substrate, wherein a cross section of each of the plurality of the first three-dimensional nano-structure, each of the plurality of second three-dimensional nano-structures, and each of the plurality of third three-dimensional nanostructures, is M-shaped.

19. The light emitting diode of claim **18**, wherein the plurality of first three-dimensional nano-structures, the plurality of second three-dimensional nano-structures, and the plurality of third three-dimensional nano-structures are distributed with a same concentration and a same alignment.

20. The light emitting diode of claim **18**, wherein the plurality of first three-dimensional nano-structures extends substantially along a first direction, and the plurality of third three-dimensional nano-structures extends substantially along a second direction, and the first direction is parallel with the second direction.

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